REMARKS

Present Status of the Application

The Office Action objected claims 5 and 6 because of informalities. The Office Action rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by Umetsu et al. (U.S. Pat. 6,424,048). Upon entry of the amendments in this response, claims 1, 5, and 6 are amended. Claims 1-6 remain pending in the present application with claim 1 being independent claim.

Claim 1 is amended by incorporating a feature that is supported by, for example, Figs.2A and the specification, paragraph [0020], lines 19-25. Claims 5 and 6 are amended to clear up matters of form. Applicants believe that the forgoing amendments do not introduce new matter. Thus, reconsideration of those claims is respectfully requested.

Objections to the claims

The Office Action objected claims 5 and 6 because of informalities. In accordance with the Examiner's request, Applicants have changed "the side edge" to " a side edge" in both of the claims. Accordingly, Applicants respectfully submit that the objection has been over come and should be withdrawn.

Rejections under 35 U.S.C. 102(b)

The Office Action rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by Umetsu et al. Applicants respectfully traverse the rejection as applied to claims 1-6 for at least the reasons set forth below.

The independent claim 1, as amended, recites as follows.

1. A vertical routing structure inside a substrate for connecting a first trace line and a second trace line electrically, wherein the substrate has a stack layer, a first patterned circuit layer, and a second patterned circuit layer, the first patterned circuit layer on a first surface of the stack layer forms the first trace line, and the second patterned circuit layer on a second surface of the stack layer forms the second trace line, the vertical routing structure comprising:

a conductive rod that passes through the stack layer such that a first surface and a corresponding second surface of the conductive rod are exposed on the first surface and the second surface of the stack layer;

a first bonding pad on the first surface of the conductive rod and formed of the first circuit layer, wherein the first bonding pad is connected to the first trace line and the transverse sectional area of the first bonding pad is smaller than the transverse sectional area of the first surface of the conductive rod; and

a second bonding pad on the second surface of the conductive rod and formed of the second circuit layer, wherein the second bonding pad is connected to the second trace line.

(emphases added)

The claimed invention disclosed that the first bonding pad and the first trace are formed of the first circuit layer on the first surface of the stack layer, and the second bonding pad and the second trace are formed of the second circuit layer on the second surface of the stack layer. Therefore, the first bonding pad and the first trace spread on the same surface (i.e. the first surface of the stack layer) without overlapping with each other, while the second bonding pad and the second trace spread on the same surface (i.e. the second surface of the stack layer) without overlapping with each other.

Umetsu et al., however, disclose in Fig. 7n that the bonding pad (between the opening in 14) and the trace line (26, part of bottom 30) do not spread on the same surface, but overlaps

with each other. Similarly, Umetsu et al. disclose in Fig. 7n that the bonding pad (between the opening in 11) and the trace line (19, part of top 30) do not spread on the same surface, but overlaps with each other.

Umetsu et al. disclose in Figs. 4A and 4B an aluminum film 12 as an electrode pad are formed on a silicon substrate 10 surface-oriented to a (100) face. The aluminum film 12 is formed on the silicon substrate 10 through an oxide film 11 and electrically connected to the device region 9 (col. 8, lines 1-6). Thus, the pad in Umetsu et al. should be a square potion of the aluminum film (12 in Figs. 4A and 4B) at the right side, but not the portions respectively between the openings in the silicon oxide films (11 or 14 in Fig. 7n). In another aspect, the trace line in Umetsu et al. should be a liner portion of the aluminum film (12 in Figs. 4A and 4B) at the left side, but not the copper layer (19, part of top 30 in Fig. 7n) or the copper layer (26, part of bottom 30 in Fig. 7n).

Umetsu et al. disclose that the semiconductor device 40 is formed from semiconductor chips 29 laminated as shown in Fig. 3, and the semiconductor chips 29 are laminated so as to be electrically connected to one another through metal bumps 30 (col. 7, lines 52-56). Thus, the pad (i.e. a square potion of the aluminum film 12 in Figs. 4A and 4B) in Fig. 7n is penetrated by the bump (30 in Fig. 7n) which forms a top terminal (19 and 25 in Fig. 7n) and a bottom terminal (20 and 26 in Fig. 7n).

Therefore, Umetsu et al. do not anticipate claim 1, as amended, since Umetsu et al. do not disclose every feature of the claim. Consequently, Umetsu et al. do not anticipate claims 2-6 as matter of law.

Accordingly, Applicant respectfully submits that the grounds of rejection have been addressed and the rejection has been overcome. Reconsideration and withdrawal of the rejection are respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-6 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 3/11/2005

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